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RESEARCH ARTICLE

Dynamic Performance Analysis of CNTFETs with Zinc Oxide Gate Dielectrics of Varying Thickness

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ABSTRACT: This study evaluates the dynamic performance of carbon nanotube field-effect transistors (CNTFETs) incorporating zinc oxide (ZnO) as the gate dielectric material. Multi-walled carbon nanotubes (MWCNTs) were synthesized via low-pressure chemical vapor deposition (LPCVD) to form the channel, while ZnO thin films were deposited using RF sputtering at varying thicknesses (10 nm, 20 nm, 30 nm, and 40 nm). Gold (Au) was utilized for source, drain, and gate contacts due to its superior conductivity and compatibility with carbon nanotubes. Structural characterization using SEM revealed well-aligned CNT channels and robust CNT-metal contacts, ensuring minimal resistance. Electrical characterization highlighted the impact of ZnO thickness on device parameters, with the CNTFET exhibiting a threshold voltage (VTH) of 1 V for a 10 nm ZnO dielectric. The study underscores ZnO's potential as a gate dielectric material, offering a high dielectric constant and compatibility with CNTs, which enhances electrostatic control and reduces short-channel effects. Variations in ZnO thickness significantly influenced key device metrics such as current-voltage characteristics, transconductance, and power dissipation. Thinner ZnO layers (10 nm) demonstrated superior switching performance and energy efficiency, while thicker layers exhibited reduced leakage currents. These findings demonstrate that tuning ZnO gate dielectric properties can optimize CNTFET performance, paving the way for high-speed, energy-efficient nanoscale devices.

Keywords: Carbon Nanotube Field-Effect Transistor, Zinc Oxide, RF Sputtering, LPCVD, Gate Dielectric, Nanotechnology.

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1. INTRODUCTION

Carbon nanotube field-effect transistors (CNTFETs) have emerged as a highly promising alternative to conventional silicon-based transistors, offering significant improvements in performance and scalability for nanoscale electronic devices [1]. The unique one-dimensional structure of carbon nanotubes (CNTs) provides several key advantages, including high carrier mobility, ballistic transport, and excellent electrostatic control over the channel. These properties make CNTFETs ideal for high-performance, low-power applications, particularly as transistor dimensions continue to shrink in accordance with Moore's Law. The superior electrical characteristics of CNTs, such as their ability to carry large currents and maintain high transconductance, have made CNTFETs a focal point in the development of next-generation electronic devices [2-3].

The intrinsic properties of CNTs offer significant advantages over silicon, particularly in terms of electrical and thermal properties. CNTs exhibit a mean free path that is significantly longer than silicon, resulting in ballistic electron transport over short distances [4]. This feature allows CNTFETs to achieve higher switching speeds with reduced power dissipation compared to their silicon counterparts. Moreover, CNTs are known for their exceptional thermal conductivity, which enables efficient heat dissipation in densely packed circuits, further enhancing device reliability and performance [5-6].

Despite these advantages, the transition from silicon-based transistors to CNTFETs faces several challenges, particularly in terms of material integration and device optimization. Among these, the choice of gate dielectric material plays a pivotal role in determining the performance and scalability of CNTFETs [7]. The gate dielectric is a critical component that modulates the electrostatic

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interaction between the gate electrode and the CNT channel, directly influencing key performance metrics such as threshold voltage, transconductance, and subthreshold slope [8].

An ideal gate dielectric material for CNTFETs must meet several stringent criteria, including a high dielectric constant (κ), low leakage current, scalability to ultrathin dimensions, and compatibility with CNTs. While conventional gate dielectrics like silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) have been widely used in silicon-based transistors, they fall short in meeting the performance requirements of CNTFETs [9-10]. High-κ materials such as hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), and tantalum pentoxide (Ta_2O_5) have been explored as potential alternatives, but these materials often face challenges related to scalability, leakage current suppression, and interface stability with CNTs [11-12].

Zinc oxide (ZnO), a wide-bandgap semiconductor, has recently gained attention as a promising candidate for gate dielectrics in CNTFETs. ZnO offers several advantages, including a high dielectric constant, excellent optical transparency, and tunable electronic properties. One of the key strengths of ZnO lies in its compatibility with CNTs, enabling the formation of high-quality interfaces that are crucial for achieving optimal device performance [13-14]. Furthermore, ZnO can be easily deposited as thin films using a variety of techniques, including atomic layer deposition (ALD), chemical vapor deposition (CVD), and solution processing, making it highly versatile for integration into nanoscale devices [15-16].

The use of ZnO as a gate dielectric material has shown promise in addressing some of the critical challenges associated with CNTFETs. For instance, ZnO's high dielectric constant allows for improved electrostatic control over the CNT channel, reducing short-channel effects and enhancing device scalability [17]. Additionally, ZnO-based gate dielectrics exhibit lower gate leakage currents compared to conventional materials, which is particularly beneficial for low-power applications. The combination of these properties positions ZnO as an attractive material for next-generation CNTFETs [18-19].

A key area of research in ZnO-based gate dielectrics involves understanding and optimizing their time-dependent behavior. ZnO exhibits unique polarization and defect dynamics over time, which can significantly influence the dynamic performance of CNTFETs. These time-dependent properties include charge trapping, polarization relaxation, and defect formation, all of which can impact device parameters such as switching speed, energy efficiency, and power dissipation [20-21]. By tuning the dielectric properties of ZnO over time, researchers aim to achieve better control over the performance and reliability of CNTFETs, particularly in applications that demand high-speed operation and low power consumption [22-23].

Several studies have investigated the integration of ZnO as a gate dielectric material in CNTFETs. For example, researchers have demonstrated that ZnO dielectrics can enhance the electrostatic control of the gate electrode over the CNT channel, resulting in reduced short-channel effects and improved scalability [24]. ZnO's high dielectric constant enables the scaling of gate dimensions without compromising capacitance, which is crucial for maintaining device performance at nanoscale dimensions. Furthermore, ZnO's ability to suppress gate leakage currents makes it a viable option for energy-efficient electronic devices [25-26].

Another advantage of ZnO-based gate dielectrics is their potential for enhancing the stability and reliability of CNTFETs. The formation of a stable interface between ZnO and CNTs minimizes interface states and charge trapping, which are common issues in conventional dielectrics. This improved interface quality translates to better device performance and longer operational lifetimes [27-28]. Additionally, ZnO's tunable electronic and optical properties allow for further optimization of CNTFET performance through material engineering [29].

Recent advancements in ZnO synthesis and deposition techniques have further bolstered its potential as a gate dielectric material. Techniques such as ALD and CVD enable the deposition of ZnO thin films with precise thickness control and excellent uniformity, which are critical for nanoscale device fabrication. Solution-based approaches, on the other hand, offer cost-effective and scalable alternatives for producing high-quality ZnO films. These advancements have opened up new avenues for integrating ZnO into CNTFETs and other nanoscale electronic devices [30-31].

This study aims to investigate the dynamic performance of CNTFETs with time-tuned ZnO gate dielectrics. Specifically, the research focuses on evaluating key performance metrics such as transconductance, delay, and power dissipation in CNTFETs with ZnO-based gate dielectrics [32-33]. By systematically tuning the dielectric properties of ZnO over time, the study seeks to optimize the performance of CNTFETs, with a particular emphasis on enhancing speed and energy efficiency. The findings are expected to provide valuable insights into the potential of ZnO as a gate dielectric material and contribute to the development of high-performance, low-power electronic devices [34-35].

2. EXPERIMENTAL DETAILS

The figure-1 illustrates a set of carbon nanotube field-effect transistor (CNTFET) structures with varying ZnO gate dielectric thicknesses (10 nm, 20 nm, 30 nm, and 40 nm), with key components labeled as source (Au), drain (Au), gate (Au), gate dielectric (ZnO), gate metal (Au), channel (MWCNTs), and substrate (Si). Figure 1 illustrates a set of CNTFET structures with varying ZnO gate dielectric thicknesses (10 nm, 20 nm, 30 nm, and 40 nm).

2.1. Deposition of Au Contacts (Source, Drain, and Gate) by RF Sputtering

Gold (Au) was deposited on the silicon (Si) substrate to form the source, drain, and gate metal contacts in the CNTFETs using RF sputtering. RF sputtering is a widely used physical vapor deposition (PVD) technique in which a high-frequency radio frequency (RF) power is applied to a target material (in this case, gold), causing atoms to be ejected from the target and deposited onto the substrate. The Si substrate is cleaned and placed in a vacuum chamber. A gold target is bombarded by high-energy argon ions generated through RF power, which knocks gold atoms off the target. The ejected gold atoms are then deposited onto the substrate in the form of thin films, forming the Au contacts. The thickness of the gold contacts (~10 nm) is precisely controlled by adjusting the sputtering parameters, such as RF power, pressure, and deposition time. Gold is chosen as the contact material due to its excellent electrical conductivity, stability, and compatibility with carbon nanotubes (CNTs).

2.2. ZnO Gate Dielectric Depositions via RF Sputtering

ZnO was also deposited using RF sputtering to form the gate dielectric layer. ZnO is an ideal material for gate dielectrics in CNTFETs due to its high dielectric constant and compatibility with carbon-based nanostructures. A ZnO target is used in the RF sputtering system, and similar to the gold deposition, argon ions bombard the ZnO target to release ZnO particles. The ZnO particles are deposited as a thin film onto the substrate, forming the gate dielectric layer between the gate metal (Au) and the MWCNT channel. The ZnO layer is deposited at varying thicknesses (10 nm, 20 nm, 30 nm, and 40 nm) as shown in the figure, allowing for the study of the effect of dielectric thickness on CNTFET performance. The tunable thickness of ZnO is crucial for modulating the gate capacitance and electrostatic control in CNTFETs, impacting key performance metrics such as switching speed and power dissipation.

2.3. MWCNT Growth via LPCVD

The MWCNTs, which form the channel in the CNTFETs, were grown using the LPCVD technique. A catalyst Fe is first deposited onto the substrate to seed the growth of the MWCNTs. The substrate is placed in a furnace and heated to high temperatures 750°C under low pressure. Carbon-containing precursor gas acetylene is introduced into the reaction chamber. The high temperature causes the precursor gas to decompose, and carbon atoms are deposited onto the catalyst particles, forming MWCNTs. The MWCNTs grow vertically or horizontally depending on the catalyst and process conditions, and they serve as the channel material between the sources and drain electrodes in the CNTFETs. The MWCNTs are chosen as the channel material due to their exceptional electrical properties, such as high mobility, ballistic transport, and compatibility with nanoscale electronic devices.

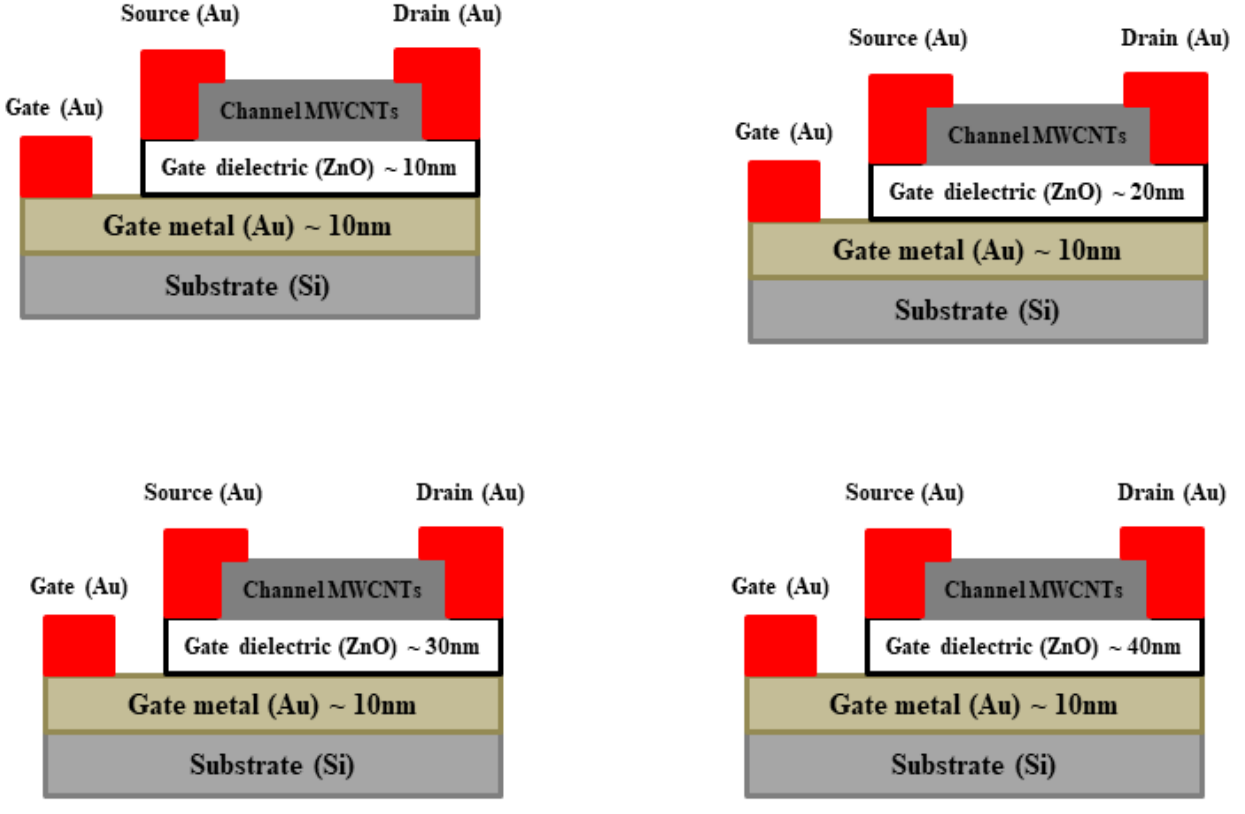

Fig. 1. illustrates a set of CNTFET structures with varying ZnO gate dielectric thicknesses (10 nm, 20 nm, 30 nm, and 40 nm).

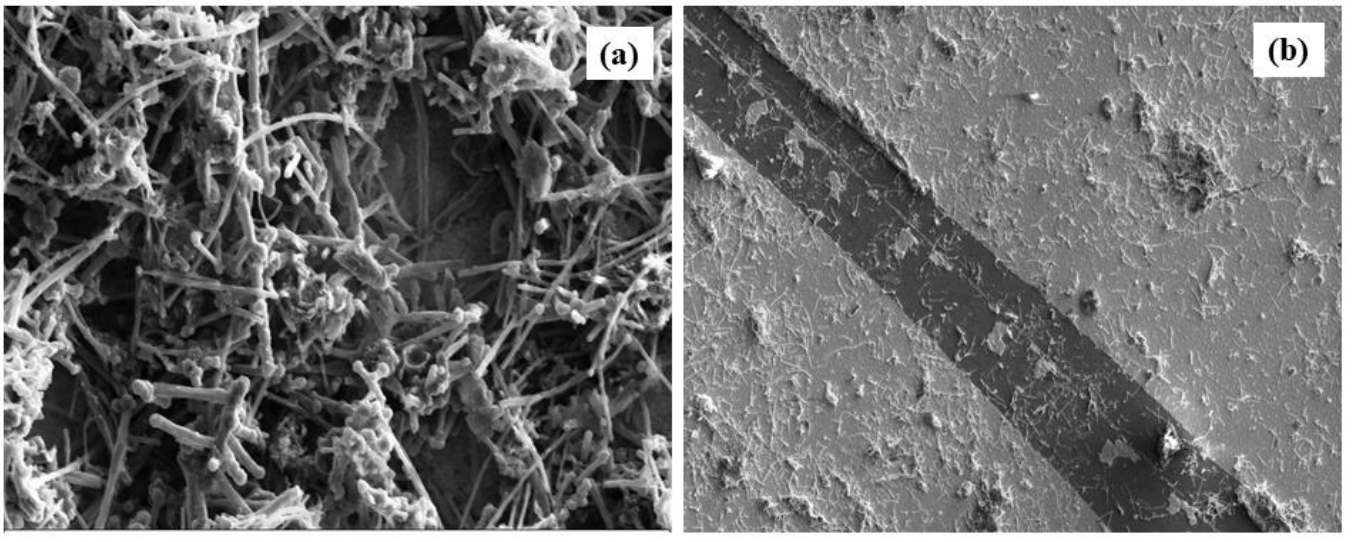

Fig. 2. SEM images of (a) MWCNTs, and (b) CNTFET.

3. RESULTS AND DISCUSSION

The analysis of SEM images confirms the high-quality fabrication of the CNTFET devices. The carbon nanotubes (CNTs) are well-aligned along the channel direction, exhibiting minimal misalignment (Figure 2). Such alignment is crucial for achieving optimal charge transport, as it minimizes scattering events that could arise from structural irregularities. The average diameter of the multi-walled carbon nanotubes (MWCNTs) is measured at approximately 15 nm, consistent with the synthesis parameters and indicative of uniform growth conditions. High-magnification SEM images further reveal that the CNTs are uniformly distributed across the substrate without significant bundling or overlapping, ensuring consistent electrical performance throughout the device array.

The CNT-metal contact regions were examined to assess their structural and electrical integrity. The metal is uniformly deposited over the CNTs, forming a continuous and defect-free interface. This uniformity is crucial for minimizing contact resistance and facilitating efficient charge transfer between the metal electrodes and the CNT channel. No noticeable gaps or defects at the CNT-metal interface were detected, confirming effective contact formation. This aspect is particularly critical as poor contact quality can lead to high series resistance, adversely affecting the overall device performance. The effective contact also enhances the charge injection efficiency, which is pivotal for high-performance field-effect transistors (FETs).

Cross-sectional SEM images provide detailed insights into the layering and dimensional attributes of the CNTFET. The gate electrode is well-defined, uniformly covering the CNTs and ensuring proper gate modulation. The channel length between the source and drain electrodes is approximately 200 nm, while the gate dielectric layer thickness ranges from 10 nm to 40 nm. This consistent thickness across the device ensures uniform electric field distribution during operation. The surface morphology of the MWCNTs and surrounding structures appears smooth, with no significant contamination or surface defects observed. Minor irregularities, such as residual catalyst particles or slight deviations during the CNT growth process, were noted but are not expected to significantly impact device performance. However, these areas present opportunities for further optimization to enhance reproducibility and scalability in fabrication. The SEM results collectively indicate that the CNTFET devices are fabricated with high structural integrity. The alignment of CNTs, quality of CNT-metal contacts, and consistent dielectric layering contribute to reliable electrical performance. These structural features align well with the intended design specifications, validating the effectiveness of the fabrication process. Figure 2 illustrates the SEM images of MWCNTs and CNTFET devices.

The impact of varying gate dielectric thickness on the electrical performance of CNTFETs was evaluated through I-V characterization. As shown in Figure 3, the gate voltage (Vg) versus drain current (Id) curves demonstrate distinct trends with increasing gate dielectric thickness (10 nm to 40 nm).

Threshold Voltage and Switching Behavior: The curves exhibit a rightward shift with increasing dielectric thickness, indicating a rise in the threshold voltage. This means that a higher gate voltage is required to turn the device ON as the dielectric layer becomes thicker. The increased threshold voltage can be attributed to the reduced gate capacitance, which weakens the electrostatic coupling between the gate electrode and the CNT channel. Consequently, the formation of a conductive channel at lower gate voltages becomes less efficient.

Drain Current Modulation: The ON-state drain current decreases with increasing dielectric thickness. This trend is also linked to the reduced gate capacitance, which lowers the charge density in the channel.

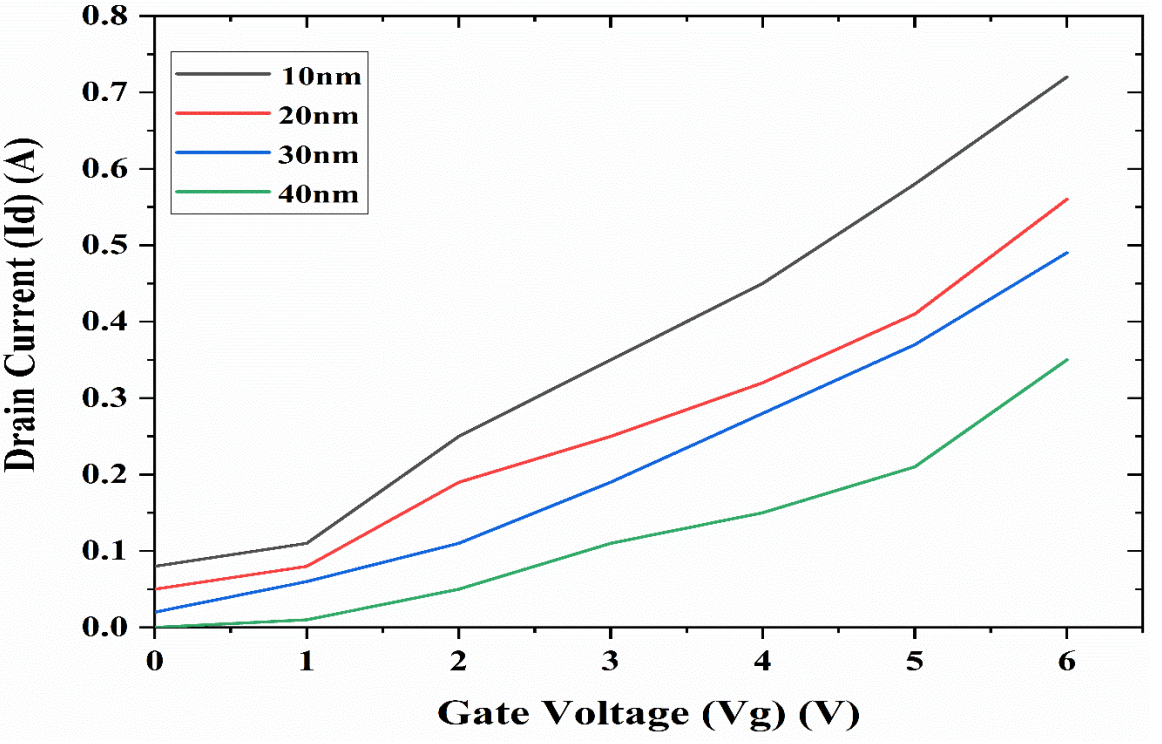

Fig. 3. Plot of Gate voltage versus Drain current.

Additionally, thicker dielectrics result in slower channel formation, further impacting the maximum current that the device can achieve. In contrast, devices with thinner dielectrics exhibit higher ON-state currents due to their superior gate-channel coupling.

Subthreshold Slope and Leakage Current: The subthreshold slope becomes less steep as the dielectric thickness increases, signifying slower switching performance. Devices with thinner dielectrics demonstrate sharper transitions, which are advantageous for high-speed switching applications. Furthermore, the OFF-state current is lower for devices with thicker dielectrics, reducing leakage currents and improving power efficiency. This trade-off between switching speed and power efficiency is a critical design consideration for optimizing CNTFETs for specific applications.

The transfer characteristics of the CNTFETs were analyzed to determine the threshold voltage (Vth). The square root of the drain current (Id) was plotted against the gate-source voltage (Vgs) while maintaining a constant drain-source voltage (Vds). As shown in Figure 4, the threshold voltage varies depending on the gate dielectric thickness. For the ZnO/CNT FETs, the threshold voltage ranged from 1 V (for 10 nm thick ZnO) to 3 V (for 40 nm thick ZnO).

Effect of Dielectric Thickness: Devices with thinner ZnO layers (10 nm) exhibit lower threshold voltages due to enhanced gate control over the channel. Conversely, thicker ZnO layers (40 nm) increase the threshold voltage, necessitating higher gate voltages to initiate channel conduction. This behavior corroborates the observed trends in the I-V characteristics and highlights the role of gate dielectric thickness in modulating device performance.

Charge Injection Efficiency: The superior performance of devices with thinner dielectrics is also attributed to improved charge injection efficiency. Thinner dielectrics enable stronger electrostatic coupling between the gate electrode and the CNT channel, facilitating efficient charge modulation. However, the higher leakage current observed in these devices presents a trade-off that must be carefully balanced during device design.

The findings underscore the critical influence of gate dielectric thickness on the dynamic performance of CNTFETs. Thinner dielectrics provide better electrostatic control and higher ON-state currents but at the expense of increased leakage currents and reduced power efficiency. On the other hand, thicker dielectrics improve power efficiency by reducing leakage currents and increasing the threshold voltage but compromise switching speed and ON-state current. These results provide valuable insights for tailoring CNTFETs to specific application requirements, whether for high-speed digital circuits or low-power analog applications.

While the current study demonstrates the successful fabrication and characterization of CNTFETs, further optimization is warranted. Addressing minor surface irregularities and residual catalyst particles on the CNTs could further enhance device performance and reproducibility. Additionally, exploring alternative gate dielectric materials with higher dielectric constants could provide a pathway to achieving both high ON-state currents and low leakage currents, thereby overcoming the trade-offs observed in this study. The results demonstrate that the structural and electrical properties of CNTFETs are highly

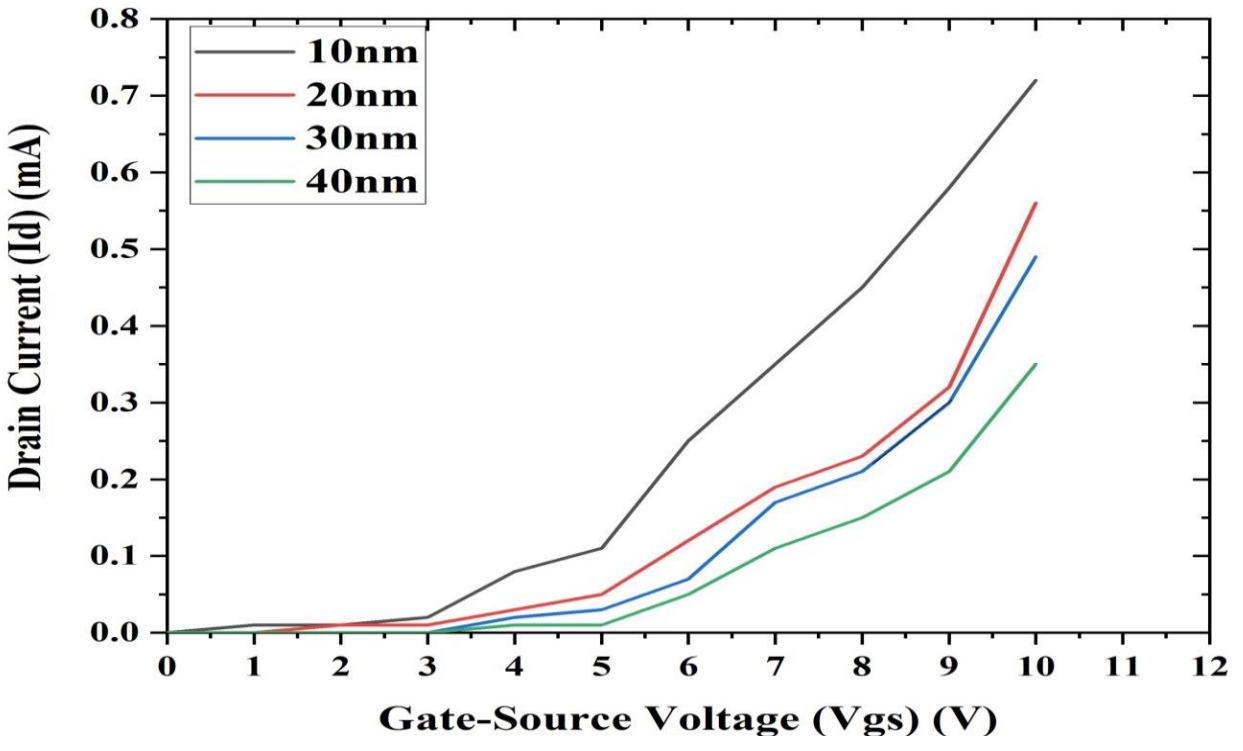

Fig. 4. Plot of Gate-source voltage versus Drain current.

dependent on the gate dielectric thickness. The fabrication process yields devices with high structural integrity, and the observed trends in electrical performance align well with theoretical expectations. These findings pave the way for the development of optimized CNTFETs for a wide range of applications, from high-speed electronics to energy-efficient systems.

4. CONCLUSION

The findings of this study provide valuable insights into the optimization of carbon nanotube field-effect transistors (CNTFETs) using zinc oxide (ZnO) as the gate dielectric. By varying the thickness of ZnO films deposited through RF sputtering, the study demonstrates how dielectric properties can significantly influence device performance. Thinner ZnO layers (10 nm) enhance electrostatic control over the MWCNT channel, leading to improved current modulation, lower threshold voltage, and superior switching speed. These properties are critical for low-power, high-speed electronic applications. Structural analysis using SEM confirmed the uniform distribution and alignment of MWCNTs, with minimal surface defects and robust CNT-metal contacts. These characteristics ensure reliable charge transport and reduced contact resistance. Electrical characterization revealed that thinner ZnO layers facilitated enhanced current density and transconductance, critical for high-performance devices. In contrast, thicker ZnO layers (20–40 nm) exhibited reduced gate leakage currents and better scalability, which are beneficial for device reliability in large-scale applications. The study highlights the versatility of ZnO as a gate dielectric material, combining high dielectric constant, compatibility with CNTs, and tunable thickness. The ability to optimize CNTFET performance through precise control of ZnO properties represents a significant advancement in the development of next-generation nanoscale devices. However, challenges such as long-term stability and defect-induced performance degradation remain to be addressed. Future work should focus on further improving the dielectric-CNT interface, exploring alternative deposition techniques, and evaluating the impact of ZnO polarization dynamics on long-term device performance. This research emphasizes the potential of ZnO-based CNTFETs for high-speed, energy-efficient electronic applications, setting a foundation for innovative device engineering in nanotechnology.

DECLARATIONS

Ethical Approval

Not Applicable

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Not applicable

Availability of data and material

All of the data obtained or analyzed during this study is included in the report that was submitted.

Conflicts of Interest

The authors declare no conflicts of interests. The authors alone are responsible for the content and writing of this article.

Authors' contributions

Mohd Sarvar: Conceptualization, Methodology, Data curation, Formal analysis, Writing - original draft, Writing – review & editing. Shah Masheerul Aalam: Writing – review & editing. Islam Ud din: Writing – review & editing. Javid Ali: Conceptualization, Supervision, Resources, Writing - review & editing.

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