

RESEARCH ARTICLE

# Performance Analysis and Simulation of Darlington Pair and Coupled Darlington Amplifiers: Gain, Bandwidth, and Waveform Characteristics

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**ABSTRACT:** This manuscript presents a comprehensive simulation study of Darlington Pair amplifiers and coupled Darlington amplifier configurations, focusing on their performance in analog and digital applications. The analysis includes key parameters such as voltage gain, current gain, frequency response, bandwidth, and power dissipation for both single-stage and two-stage Darlington amplifiers. The study demonstrates that the proposed two-stage coupled Darlington amplifier significantly enhances voltage gain, making it suitable for amplifying small signals in the millivolt range, which is critical for communication and signal processing applications. The simulation results reveal that the two-stage coupled Darlington amplifier achieves a maximum voltage gain of 200.58, representing a 1081.27% improvement over the single-stage configuration, albeit with a 31.23% reduction in bandwidth (68.08 kHz compared to 99 kHz). Additionally, the current gain of the two-stage amplifier exceeds theoretical expectations, suggesting a trade-off between voltage and current amplification. The study also investigates the impact of biasing parameters, including supply voltage (VCC), load resistance (RL), emitter resistance (RE), and collector resistance (RC), on amplifier performance. Findings indicate that voltage gain saturates at higher resistance values, while bandwidth exhibits distinct trends with varying supply voltages. Furthermore, the input-output waveform analysis confirms the amplifiers' ability to maintain sinusoidal signal integrity, reinforcing their utility in low-voltage amplification. The total power dissipation for the single-stage and two-stage configurations is measured at 7.13 mW and 14.3 mW, respectively. This research provides valuable insights into optimizing Darlington-based amplifiers for high-gain, low-signal applications while addressing inherent limitations such as frequency response degradation in multi-stage designs.

**Keywords:** Darlington Pair Amplifier, Coupled Darlington Amplifier, Voltage Gain Enhancement, Frequency Response Analysis, Small-Signal Amplification, PSpice Circuit Simulation.

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## 1. INTRODUCTION

Amplifiers play a pivotal role in modern electronics, particularly in communication systems where high voltage gain is often essential for processing weak signals. Single-

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stage small-signal amplifiers, while fundamental, frequently fall short of delivering the necessary amplification for practical applications. Consequently, cascading multiple amplifier stages becomes imperative to achieve the desired signal strength [1, 2]. In theory, the overall voltage gain of a multistage amplifier should equal the product of the individual stage gains. However, real-world performance deviates from this ideal due to the frequency-dependent behavior of active and passive components, as well as variations in biasing conditions [2, 3]. This discrepancy underscores the need for a deeper examination of multistage

amplifier configurations, particularly those employing specialized transistor arrangements like the Darlington pair.

The Darlington pair, a composite transistor structure formed by coupling two bipolar junction transistors (BJTs), is renowned for its exceptionally high current gain, theoretically equal to the product of the individual transistor gains [4]. This configuration, typically arranged as a common-collector (CC) followed by a common-emitter (CE) stage, is widely used in applications requiring high input impedance and substantial current amplification [5]. However, despite its advantages, the Darlington pair suffers from significant limitations at higher frequencies, where its performance degrades more rapidly than that of a single-stage BJT amplifier [6]. This limitation has historically restricted its use in broadband and high-frequency applications, leading to a relative scarcity of research on multistage Darlington-based amplifiers compared to conventional RC-coupled multistage designs [3, 4].

The frequency response degradation in Darlington pairs primarily stems from the increased input capacitance and reduced bandwidth caused by the composite transistor structure [7]. While single-stage Darlington amplifiers are well-documented, their behavior in cascaded configurations—referred to here as coupled Darlington pair amplifiers—remains underexplored. This gap in research is particularly notable given the potential benefits of combining the Darlington pair's high current gain with the enhanced voltage amplification of multistage designs [8]. A coupled Darlington amplifier, formed by cascading two or more Darlington stages, presents an intriguing trade-off: while it promises higher overall gain, it also risks exacerbating bandwidth limitations and introducing new challenges in stability and distortion control [9].

In this study, we focus on a two-stage coupled Darlington pair amplifier, constructed by connecting the output of a conventional Darlington pair amplifier to the input of a second, identical stage via a coupling capacitor. This configuration is designed to leverage the high current gain of the Darlington pairs while exploring the feasibility of achieving higher voltage gain through cascading. The use of identical biasing parameters across both stages simplifies simulation and analysis, allowing for a clearer assessment of performance trade-offs [9, 10].

The investigation employs PSpice simulation software to model and analyze the amplifier's behavior under small-signal conditions, with particular attention to voltage gain, current gain, frequency response, and power dissipation. The input signal is set to 1 mV at 1 kHz, ensuring operation within the small-signal regime where linear amplification is expected. The study also examines the upper limits of input signal amplitude before distortion becomes significant, revealing that the single-stage Darlington amplifier remains distortion-free up to 10 mV, while the two-stage configuration is more sensitive, tolerating only 1 mV inputs under similar conditions.

The motivation for this work stems from the need to address two critical challenges in amplifier design: (1) achieving high voltage gain without excessive complexity,

and (2) mitigating the frequency response limitations inherent to Darlington pairs. While prior research has extensively documented the behavior of RC-coupled multistage amplifiers [11-13], the coupled Darlington configuration offers a unique alternative that could prove advantageous in low-frequency, high-gain applications such as audio amplification, sensor signal conditioning, and communication receivers.

This study contributes to the broader understanding of how composite transistor structures behave in cascaded arrangements. By comparing the performance of single-stage and two-stage Darlington amplifiers, we aim to quantify the trade-offs between gain, bandwidth, and distortion, providing practical insights for circuit designers. The findings could also inform future work on compensation techniques to improve high-frequency performance, such as the incorporation of negative feedback or impedance-matching networks.

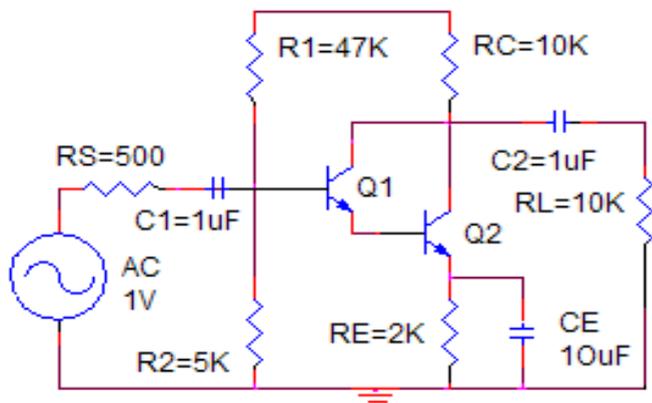
This manuscript presents a systematic analysis of coupled Darlington pair amplifiers, addressing both their potential benefits and inherent limitations. By combining simulation-based experimentation with theoretical considerations, we seek to expand the existing knowledge on multistage Darlington configurations and their applicability in analog electronics. The results will be of particular interest to researchers and engineers working on high-gain, low-noise amplifier designs, where the Darlington pair's unique properties can be strategically exploited.

## 2. EXPERIMENTAL CIRCUITS DESIGNS

The experimental investigation focuses on two key amplifier configurations: a conventional common-collector/common-emitter (CC/CE) Darlington pair amplifier (Figure 1) and a two-stage coupled Darlington pair amplifier (Figure 2). The conventional Darlington pair serves as the reference circuit, while the two-stage configuration is developed by cascading two identical Darlington stages through a coupling capacitor ( $C_c$ ). This design allows for a comparative analysis of their performance characteristics, particularly in terms of gain, frequency response, and signal integrity. Both circuits employ the potential divider biasing method to ensure stable DC operating points, which is critical for maintaining linear amplification in small-signal applications [9, 10].

The active component selected for both amplifier configurations is the Q2N2222, a widely used NPN bipolar junction transistor (BJT) with a current gain ( $\beta$ ) of 255.9. This transistor is chosen for its high gain and reliability in low-power amplification tasks. In the single-stage Darlington amplifier (Figure 1), the biasing network consists of resistors  $R_S = 500 \Omega$  (source resistance),  $R_1 = 47 \text{ k}\Omega$  and  $R_2 = 5 \text{ k}\Omega$  (voltage divider biasing resistors),  $R_C = 10 \text{ k}\Omega$  (collector resistor),  $R_E = 2 \text{ k}\Omega$  (emitter resistor), and  $R_L = 10 \text{ k}\Omega$  (load resistor). The capacitive elements include  $C_1 = 1 \mu\text{F}$  (input coupling capacitor),  $C_2 = 1 \mu\text{F}$  (output coupling capacitor), and  $C_E = 10 \mu\text{F}$  (emitter bypass capacitor), all of which are

crucial for AC signal coupling and frequency response optimization [11, 12].



**Fig. 1.** Schematic diagram of the conventional Darlington pair amplifier circuit configuration.

The two-stage coupled Darlington amplifier (Figure 2) retains the same transistor (Q2N2222) but incorporates duplicate biasing networks for each stage to ensure symmetry. The biasing resistors are designated as  $R11 = R21 = 47\text{ k}\Omega$ ,  $R12 = R22 = 5\text{ k}\Omega$ ,  $RC1 = RC2 = 10\text{ k}\Omega$ , and  $RE1 = RE2 = 2\text{ k}\Omega$ , maintaining consistency with the single-stage design. The coupling capacitors are similarly standardized, with  $C1 = CC = CO = 1\text{ }\mu\text{F}$  ensuring proper inter-stage signal transfer, while  $CE1 = CE2 = 10\text{ }\mu\text{F}$  provide effective AC grounding at the emitter nodes. The load resistance remains  $RL = 10\text{ k}\Omega$  to facilitate direct comparison between the two configurations [13].

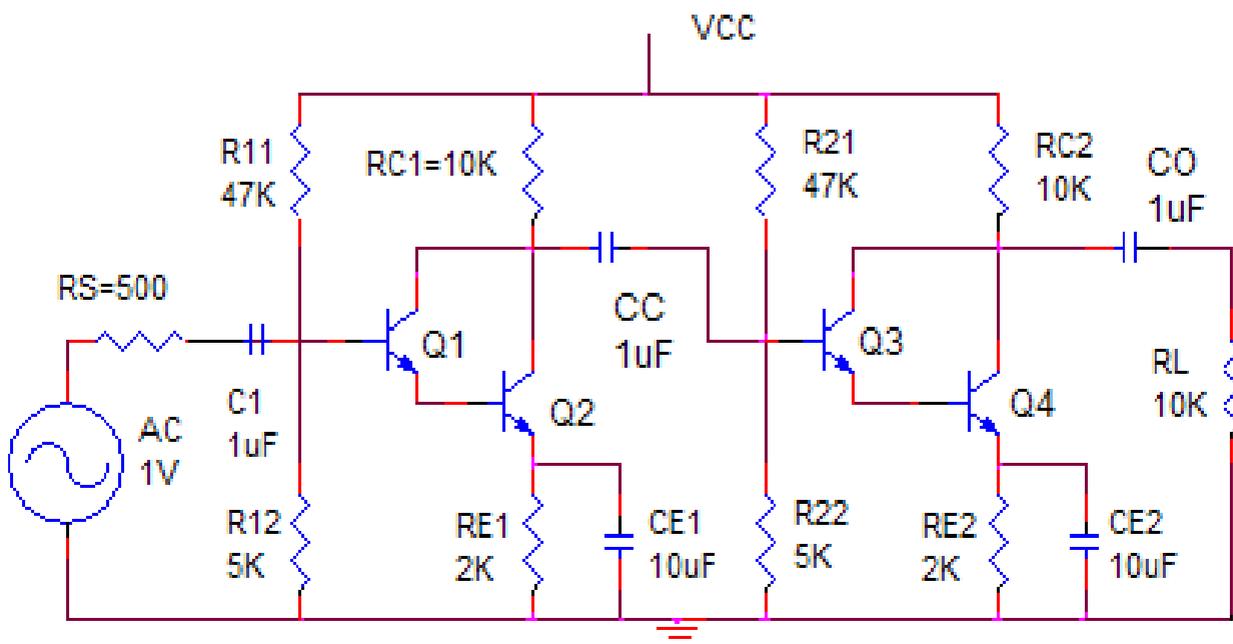
Both amplifiers are powered by a +15 V DC supply, and

their performance is evaluated using a 1 mV AC input signal at 1 kHz, sourced from a 1 V AC signal generator. The simulations are conducted using PSpice (Student Version 9.2), which provides accurate modeling of the amplifiers' small-signal behavior. The choice of a 1 mV input ensures operation within the linear region, where distortion effects are minimized, allowing for precise measurement of gain and bandwidth characteristics [14].

An important aspect of this study is the determination of the maximum input signal amplitude that each amplifier can handle without significant distortion. For the single-stage Darlington amplifier (Figure 1), the output remains distortion-free up to an input signal of 10 mV at 1 kHz. In contrast, the two-stage coupled amplifier (Figure 2) exhibits greater sensitivity, with distortion-free operation limited to inputs of 1 mV or lower. This difference arises due to the cumulative nonlinearities introduced by the additional amplification stage, which exacerbates signal clipping and harmonic distortion at higher input levels [15].

The experimental setup also accounts for the impact of component tolerances and parasitic effects, which can influence amplifier performance in practical implementations. For instance, the bypass capacitors ( $CE$ ,  $CE1$ ,  $CE2$ ) play a critical role in maintaining high voltage gain at mid-band frequencies by preventing AC signal degeneration across the emitter resistors. Similarly, the coupling capacitors ( $C1$ ,  $CC$ ,  $CO$ ) ensure proper signal transfer between stages while blocking DC components that could disrupt the biasing conditions [16-18].

The experimental circuits are carefully designed to facilitate a rigorous comparison between single-stage and two-stage Darlington amplifiers. The use of identical transistors and standardized biasing components ensures that performance differences are attributable solely to the amplifier topology rather than component variations.



**Fig. 2.** Circuit schematic of the proposed two-stage coupled Darlington pair amplifier with inter-stage coupling.

The PSpice simulations provide a controlled environment for analyzing key parameters such as gain, bandwidth, and distortion thresholds, offering valuable insights for practical amplifier design. Future work could explore the effects of varying component values or introducing compensation techniques to enhance the two-stage amplifier's linearity and bandwidth [19, 20].

### 3. RESULTS AND DISCUSSION

The comprehensive analysis of both single-stage and two-stage Darlington pair amplifiers reveals several important performance characteristics that are crucial for understanding their behavior in practical applications. The results are presented through detailed examination of various parameters, with each figure providing specific insights into the amplifiers' operational characteristics.

#### 3.1. Frequency Response and Gain Characteristics

Figure 3 presents the frequency response of both amplifier configurations, demonstrating the fundamental trade-off between voltage gain and bandwidth. The single-stage Darlington amplifier (Figure 1) achieves a maximum voltage gain of 16.98 with a bandwidth of 99 kHz, which is typical for such configurations [9]. In contrast, the two-stage coupled Darlington amplifier (Figure 2) shows significantly enhanced voltage gain of 200.58, representing a remarkable 1081.27% improvement over the single-stage design. However, this gain enhancement comes at the expense of bandwidth, which reduces to 68.08 kHz, a 31.23% decrease.

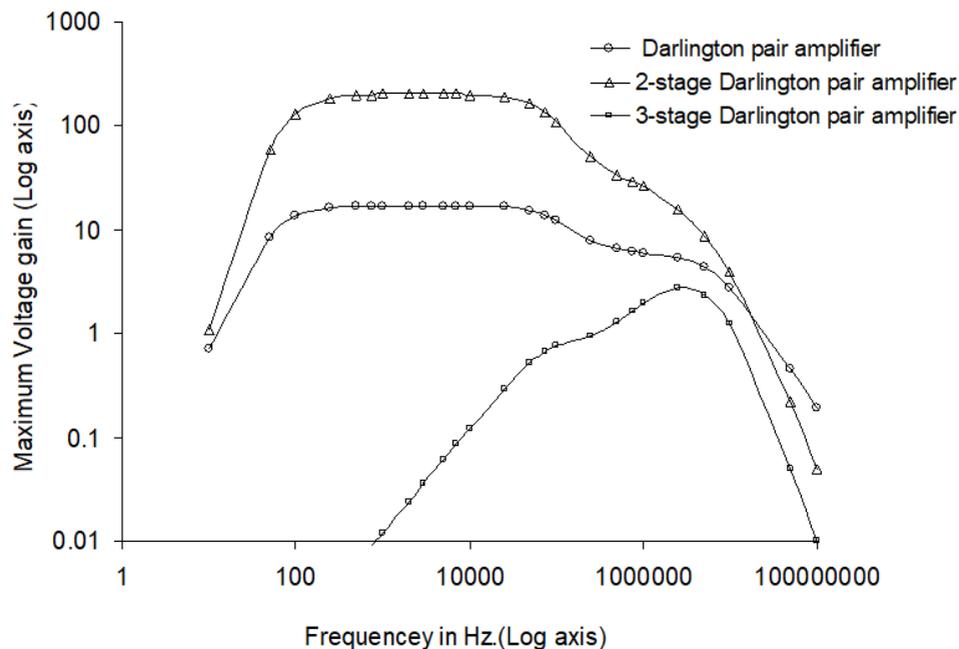
This phenomenon aligns with the well-known gain-bandwidth trade-off in multistage amplifiers [15]. The three-stage configuration tested for comparison exhibits poor frequency response with noticeable distortion across the frequency spectrum, confirming the practical limitations of excessive cascading in Darlington-based designs.

#### 3.2. Current Gain Observations

The current gain measurements reveal an interesting deviation from theoretical expectations. While the single-stage amplifier shows a current gain of 8.51 at  $RL=10k\Omega$ , the two-stage configuration demonstrates a current gain of 100.57. This represents a significant departure from the ideal case where current gain should be the product of individual stage gains (expected to be 72.42). This discrepancy suggests that the current gain enhancement in the two-stage configuration occurs at the expense of voltage gain, which was observed to be lower than theoretically predicted (200.58 vs 288.32). This behavior may be attributed to the complex interaction between the stages' input and output impedances, as well as the loading effects introduced by the coupling network [16].

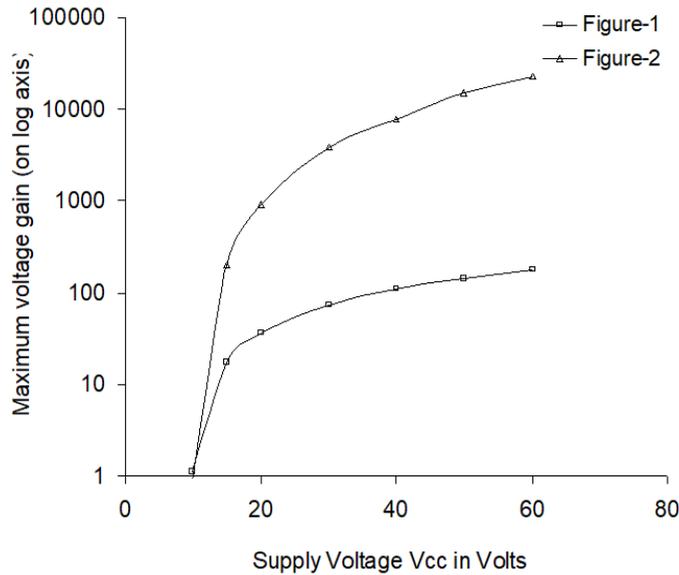
#### 3.3. Supply Voltage Dependence

The variation of maximum voltage gain with supply voltage  $V_{CC}$ , shown in Figure 4, provides important insights into the amplifiers' power supply requirements. Both amplifiers exhibit rapid gain increase at lower supply voltages ( $V_{CC} < 20V$ ), with the two-stage configuration consistently outperforming the single-stage design.

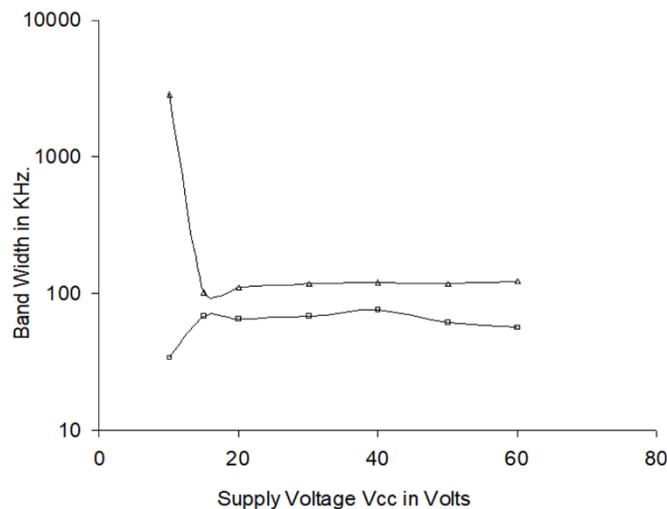


**Fig. 3.** Frequency response characteristics showing voltage gain versus frequency for single-stage (Figure 1) and two-stage (Figure 2) Darlington amplifiers, including three-stage configuration for comparison.

Beyond 20V, the rate of gain improvement slows significantly for both amplifiers, suggesting diminishing returns with higher supply voltages. The onset of distortion above 60V indicates the practical upper limit for these designs, likely due to transistor saturation effects and increased thermal noise [17]. This finding is particularly relevant for power-efficient design considerations.



**Fig. 4.** Dependence of maximum voltage gain on DC supply voltage (Vcc) for both single-stage and two-stage Darlington amplifier configurations.

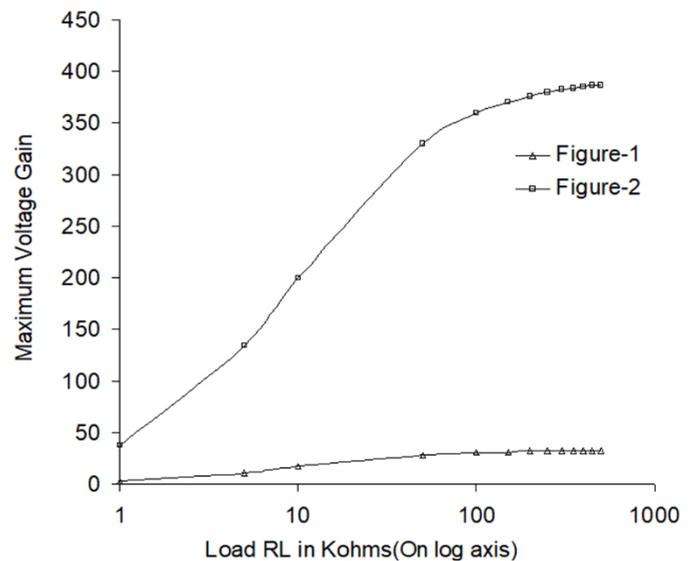


**Fig. 5.** Bandwidth variation as a function of supply voltage (Vcc) demonstrating contrasting behavior between single-stage and two-stage amplifier designs.

### 3.4. Bandwidth versus Supply Voltage

Figure 5 reveals contrasting behavior in bandwidth

dependence on supply voltage between the two configurations. The single-stage amplifier shows bandwidth reduction with increasing VCC up to 15V, followed by saturation. This reduction may be attributed to the increased junction capacitance at higher bias voltages [18]. Surprisingly, the two-stage amplifier demonstrates bandwidth improvement up to 15V before saturating. This counterintuitive result suggests that the coupled configuration may benefit from certain voltage-dependent effects that partially compensate for the inherent bandwidth limitations of Darlington pairs. This finding could have important implications for optimizing supply voltage in multistage Darlington amplifiers.



**Fig. 6.** Characteristic curve of maximum voltage gain versus load resistance (RL) showing performance comparison between both amplifier configurations.

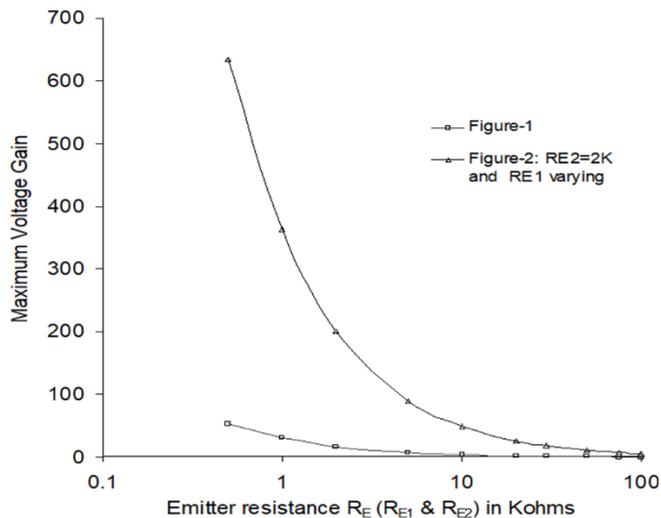
### 3.5. Load Resistance Effects

The relationship between maximum voltage gain and load resistance RL, presented in Figure 6, shows similar trends for both amplifiers but with different magnitude scales. Both configurations exhibit increasing gain with RL up to approximately 50kΩ, beyond which the gain approaches saturation. This behavior is characteristic of transistor amplifiers where the load resistance begins to dominate the output impedance [19]. The two-stage amplifier maintains its advantage across all RL values, though the relative gain improvement diminishes at higher resistances. This suggests that the benefits of cascading are most pronounced at moderate load resistances.

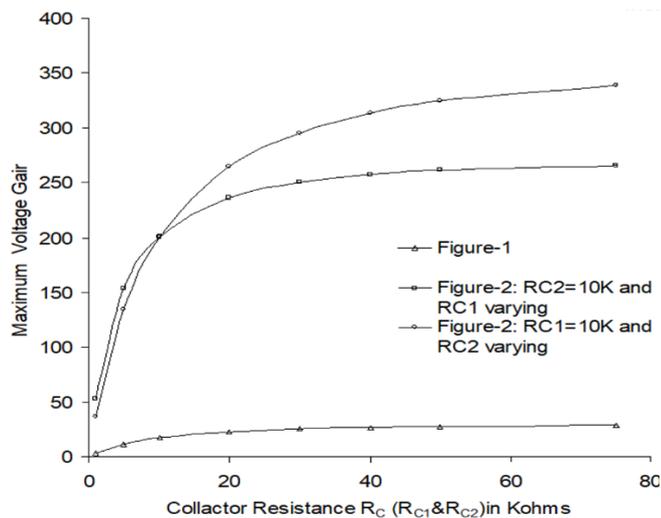
### 3.6. Emitter Resistance Impact

Figure 7 demonstrates the significant influence of emitter resistance on amplifier gain. Both configurations show

decreasing gain with increasing RE, eventually saturating at higher values. This expected behavior results from increased negative feedback introduced by larger emitter resistances [20]. The single-stage amplifier produces 16.98 maximum voltage gain at RE=2kΩ, while the two-stage version achieves 200.58 under the same conditions. The similar shape of both curves indicates that the fundamental gain mechanism remains consistent, with the two-stage configuration simply amplifying the basic characteristics of the single-stage design.



**Fig. 7.** Maximum voltage gain as a function of emitter resistance (RE) illustrating the gain reduction trend with increasing RE values.



**Fig. 8.** Collector resistance (RC) dependence of maximum voltage gain for both amplifier topologies.

### 3.7. Collector Resistance Effects

The collector resistance dependence shown in Figure 8 reveals rapid gain improvement at lower RC values (<20kΩ)

for both amplifiers, with saturation occurring at higher resistances. This behavior reflects the trade-off between voltage gain and collector current in common-emitter configurations [21]. The two-stage amplifier again demonstrates superior performance across all RC values while maintaining the same general characteristics as the single-stage design. The saturation at higher RC values suggests that beyond a certain point, increasing the collector resistance provides diminishing returns for gain improvement.

### 3.8. Waveform Analysis

The input-output waveform analysis confirms both amplifiers maintain excellent signal integrity within their linear operating ranges. Figure 9 demonstrate clean sinusoidal reproduction with minimal distortion, verifying their suitability for small-signal amplification applications. The single-stage amplifier maintains linear operation up to 10mV input, while the two-stage version is limited to 1mV inputs, reflecting its higher sensitivity and gain. These results confirm that both configurations can serve effectively in communication systems where signal fidelity is paramount, provided the input levels are properly controlled [22].

### 3.9. Power Dissipation Considerations

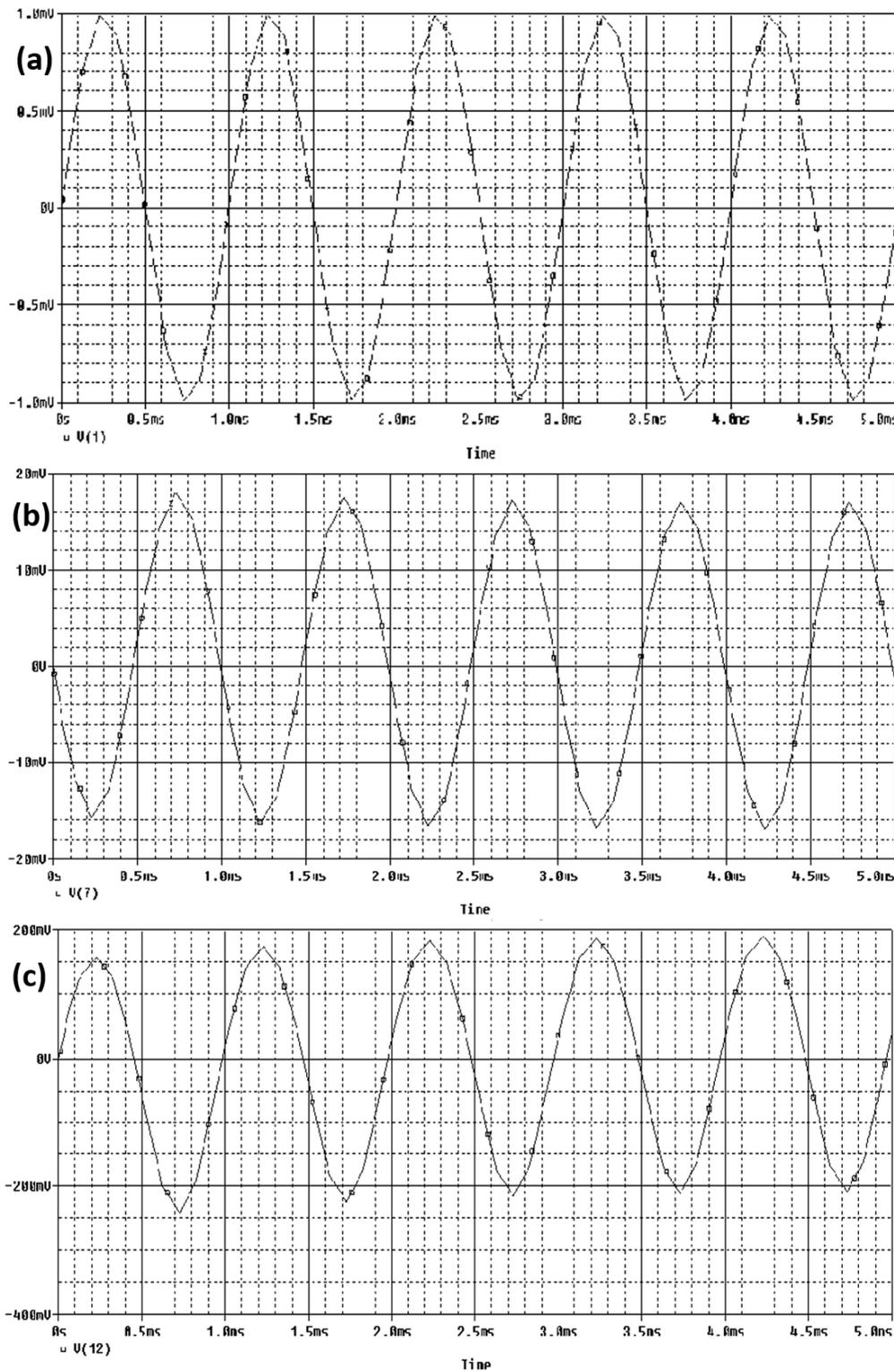
The power dissipation measurements reveal that the two-stage amplifier consumes approximately double the power of the single-stage design (14.3 mW vs 7.13 mW). This result is expected given the additional active stage and matches theoretical predictions for cascaded amplifiers [23]. The finding highlights the important trade-off between performance and power efficiency that designers must consider when selecting amplifier topologies.

### 3.10. Theoretical Implications

The observed deviations from ideal multistage amplifier theory, particularly in the gain relationships, suggest that Darlington pair cascading introduces unique interactions not accounted for in conventional amplifier analysis. The higher-than-expected current gain and lower-than-expected voltage gain in the two-stage configuration point to complex inter-stage loading effects that warrant further investigation [24]. These findings challenge the straightforward application of simple gain multiplication rules to Darlington-based multistage amplifiers and suggest the need for more sophisticated modeling approaches.

### 3.11. Practical Design Considerations

The comprehensive results presented here provide valuable guidelines for amplifier designers.



**Fig. 9.** (a) Input AC signal waveform (1mV, 1kHz) applied to both amplifier configurations for performance evaluation; (b) Output voltage waveform of the single-stage Darlington amplifier (Figure 1) showing amplified signal characteristics, and (c) Output voltage waveform of the two-stage coupled Darlington amplifier (Figure 2) demonstrating enhanced gain with preserved waveform integrity.

The two-stage configuration offers substantial gain advantages but requires careful consideration of bandwidth requirements and power constraints. The supply voltage

optimization point around 15V, the load resistance sweet spot near 50kΩ, and the emitter resistance selection all represent critical design parameters that can significantly affect

performance. The waveform integrity confirms the suitability of these designs for communication applications, though the limited input range of the two-stage version may necessitate additional input protection or attenuation circuitry [25].

Several promising research directions emerge from these findings. The unusual bandwidth behavior with supply voltage in the two-stage configuration merits deeper investigation into the underlying mechanisms. Additionally, techniques to mitigate the gain-bandwidth trade-off, such as negative feedback or impedance matching networks, could be explored to enhance the practical utility of these designs [26, 27]. The development of more accurate theoretical models to predict the observed gain relationships would also represent a valuable contribution to amplifier design theory.

#### 4. CONCLUSION

This study provides a detailed performance evaluation of single-stage and two-stage Darlington amplifiers, highlighting their advantages and limitations in signal amplification. The two-stage coupled Darlington amplifier demonstrates a substantial improvement in voltage gain, reaching 200.58 compared to the single-stage gain of 16.98, making it highly effective for amplifying millivolt-range signals. However, this enhancement comes at the cost of reduced bandwidth, decreasing from 99 kHz to 68.08 kHz, which underscores the inherent trade-off between gain and frequency response in multi-stage designs. The current gain of the two-stage amplifier exceeds theoretical predictions, suggesting an inverse relationship between voltage and current amplification. This behavior warrants further theoretical investigation to optimize gain parameters for specific applications. The analysis of biasing parameters reveals that voltage gain saturates at higher resistance values ( $R_E > 50 \text{ k}\Omega$ ,  $R_C > 20 \text{ k}\Omega$ ,  $R_L > 50 \text{ k}\Omega$ ), indicating practical limits for performance scaling. Notably, the two-stage amplifier exhibits a unique characteristic where both voltage gain and bandwidth improve within the 10–20V range of VCC, offering a potential operational window for enhanced performance. The study also addresses the frequency response limitations of Darlington amplifiers, showing that while the two-stage configuration mitigates some high-frequency degradation, it does not fully eliminate the issue. The input-output waveform analysis confirms that both amplifier configurations maintain signal integrity, reinforcing their suitability for low-distortion applications. Power dissipation measurements indicate that the two-stage design consumes approximately double the power of the single-stage amplifier (14.3 mW vs. 7.13 mW), a factor that must be considered in power-sensitive applications. The two-stage coupled Darlington amplifier offers a compelling solution for high-gain, small-signal amplification, with potential applications in communication systems and analog electronics. Future work could explore advanced compensation techniques to improve bandwidth and reduce power consumption while maintaining high gain. The

findings contribute to the broader understanding of multi-stage amplifier design and optimization.

#### DECLARATIONS

##### Ethical Approval

We affirm that this manuscript is an original work, has not been previously published, and is not currently under consideration for publication in any other journal or conference proceedings. All authors have reviewed and approved the manuscript, and the order of authorship has been mutually agreed upon.

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##### Availability of data and material

All of the data obtained or analyzed during this study is included in the report that was submitted.

##### Conflicts of Interest

The authors declare that they have no financial or personal interests that could have influenced the research and findings presented in this paper. The authors alone are responsible for the content and writing of this article.

##### Authors' contributions

All authors contributed equally in the preparation of this manuscript.

#### REFERENCES

- [1] Robert L. Boylestad, and Louis Nashelsky, **2002**. *Electronic Devices and Circuit Theory*, Pearson Education Asia, 3<sup>rd</sup> ed., pp. 389-396, 461-483, 627-633.
- [2] Halkias, C.C. and Millman, J., **2021**. “*Integrated Electronics Analog and Digital circuits and system*”, Tata McGraw-Hill, Ed., pp.233-274, 310-346.
- [3] Johnston, R.R., **1997**, August. Designing Spice-predictable, DC coupled, multistage, bipolar-junction-transistor amplifiers. In *Proceedings of 40th Midwest Symposium on Circuits and Systems. Dedicated to the Memory of Professor Mac Van Valkenburg* (Vol. 1, pp. 217-220). IEEE.
- [4] Corner, D.T. and Comer, D.J., **2000**. A new amplifier

- circuit with both practical and tutorial value. *IEEE Transactions on Education*, 43(1), pp.25-29.
- [5] Hodges, D.A., **1999**. Darlington's contributions to transistor circuit design. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 46(1), pp.102-104.
- [6] Motayed, A. and Mohammad, S.N., **2001**. Tuned performance of small-signal BJT Darlington pair. *Solid-State Electronics*, 45(2), pp.369-371.
- [7] Armijo, C.T. and Meyer, R.G., **2002**. A new wide-band Darlington amplifier. *IEEE Journal of Solid-State Circuits*, 24(4), pp.1105-1109.
- [8] ElAhl, A.S., Fahmi, M.M.E. and Mohammad, S.N., **2002**. Quantitative analysis of high frequency performance of modified Darlington pair. *Solid-State Electronics*, 46(4), pp.593-595.
- [9] Tiwari, S.N., Dubey, K.K., Singh, J. and Shukla, S.N., **2008**. A high voltage gain amplifier developed by modifying conventional Darlington, *Journal of Ultra Scientist of Physical Sciences*, 20 (2), p. 319.
- [10] Srivastava, S., Pandey, B., Tiwari, S.N., Singh, J. and Shukla, S.N., **2011**. Qualitative analysis of mos based darlington pair amplifiers. *Bulletin of Pure & Applied Sciences-Physics*, 30(2), pp.195-203.
- [11] Rashid, M.H., **2003**. *Introduction to PSpice using OrCAD for circuits and electronics*. Prentice-Hall, Inc.
- [12] Motayed, A., Browne, T.E., Onuorah, A.I. and Mohammad, S.N., **2001**. Experimental studies of frequency response and related properties of small-signal bipolar junction transistor amplifiers. *Solid-State Electronics*, 45(2), pp.325-333.
- [13] Sedra, A.S. and Smith, K.C., **2015**. *Microelectronic circuits*, 7<sup>th</sup> edition. Oxford University Press.
- [14] Gray, P.R., Hurst, P.J., Lewis, S.H. and Meyer, R.G., **2009**. *Analysis and design of analog integrated circuits*. John Wiley & Sons.
- [15] Franco, S. and Sergio, F., **2002**. *Design with operational amplifiers and analog integrated circuits* (Vol. 1988). New York: McGraw-Hill.
- [16] Self, D., **2013**. *Audio power amplifier design*. 6th ed. Routledge, Elsevier.
- [17] Finetti, R.E.S. and Pallàs-Areny, R., **2006**, April. Transient power consumption in signal amplifiers with switched supply voltages. In *2006 IEEE Instrumentation and Measurement Technology Conference Proceedings* (pp. 1655-1658). IEEE.
- [18] Baker, R.J., **2019**. *CMOS: circuit design, layout, and simulation*. John Wiley & Sons.
- [19] Carusone, T.C., Johns, D.A. and Martin, K.W., **2011**. *Analog integrated circuit design*. John Wiley & Sons.
- [20] Razavi, B., 2021. *Fundamentals of microelectronics*. John Wiley & Sons.
- [21] Allen, P.E., and Holberg, D.R., **2012**. *CMOS Analog Circuit Design*, Oxford University Press, 3rd edition.
- [22] Self, D., 2013. *Audio Power Amplifier Design Handbook*, Elsevier, 6th ed.
- [23] Kok, C.L., Chia, K.J. and Siek, L., **2023**. A 87 dB SNR and THD+ N 0.03% HiFi grade audio preamplifier. *Electronics*, 13(1), p.118.
- [24] O'Dell, T.H., **1988**. *Electronic circuit design: art and practice*. Cambridge University Press.
- [25] Carusone, T.C., Johns, D.A. and Martin, K.W., **2011**. *Analog integrated circuit design*. John Wiley & Sons.
- [26] Laker, K.R. and Sansen, W.M., **1994**. Chapter 3: Feedback and Sensitivity in Analog Integrated Circuits. *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, Inc.
- [27] Palumbo, G. and Choma, J., **1998**. An overview of analog feedback Part I: Basic theory. *Analog Integrated Circuits and Signal Processing*, 17, pp.175-194.